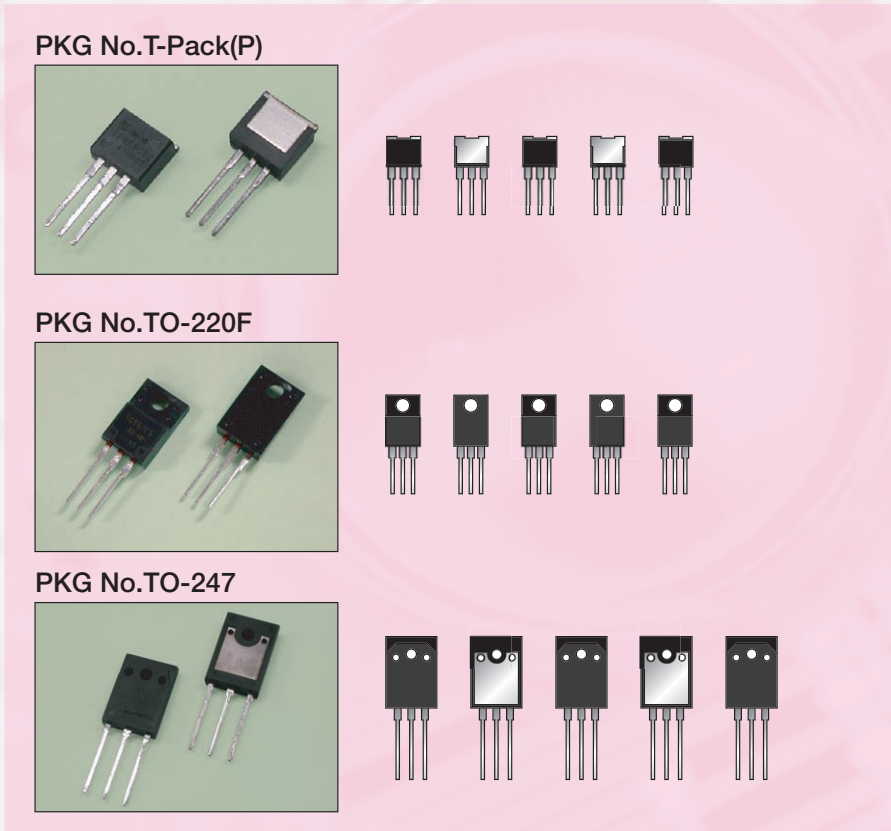


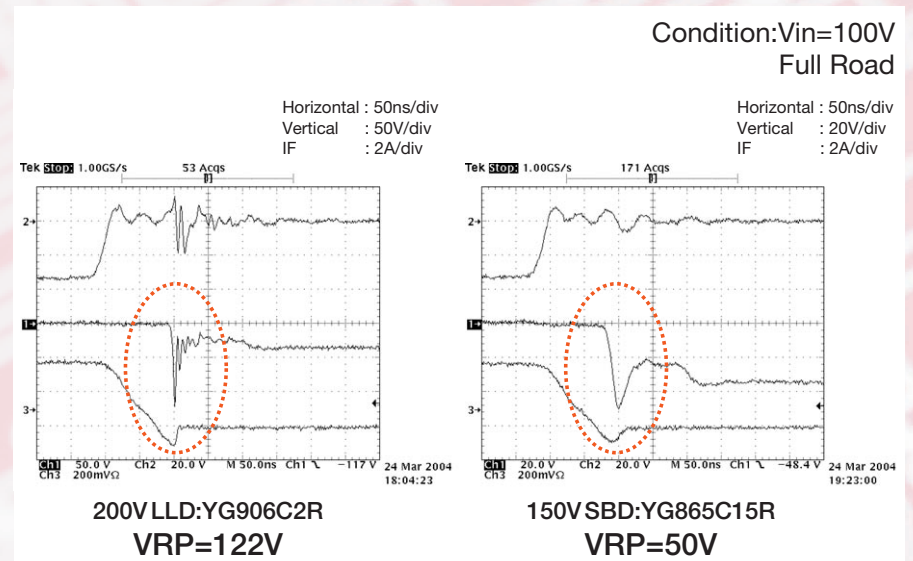
富士高压 SBD

Fuji High Voltage SBD



台式电脑12V输出电路评价结果

Evaluation results of D/T PC 12V output circuit



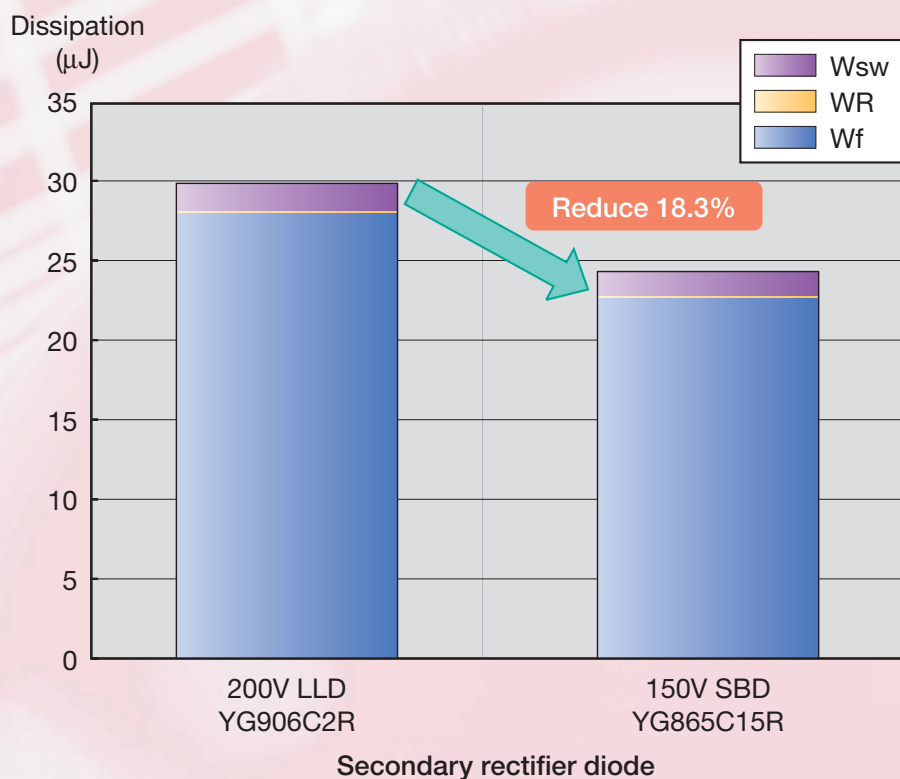
- ① LLD VRP=122V → SBD VRP=50V
: Decrease about 60%
Low Noise and Soft Recovery
- ② LLD $\Delta T_c=90\text{deg}$ → SBD $\Delta T_c=78\text{deg}$
: Decrease 12deg /Low temperature

特性 Features

- Low Noise and Low Surge Voltage
 - (1) dv/dt: 1/5 Conventional Type
⇒ A reduction of Noise Measure Parts and Snubber Circuit
 - (2) Lower Voltage SBD can be applied
- Low dissipation
 - (1) Low dissipation: reduce 20% conventional type
⇒ miniaturize heat sink reduction parallel parts numbers
miniaturize package size

12V输出电路计算结果

Calculation results of 12V output circuit



系列表：高压SBD

Line-up plan: High voltage SBD

V _{RRM} (V)	Package	I _o (A)		
		10	20	30
120	TO-220	YA862C12R	YA865C12R	YA868C12R
	TO-220F	YG862C12R	YG865C12R	YG868C12R
	T-Pack(D2)	TS862C12	TS865C12	—
	TFP	MS862C12	MS865C12	—
150	TO-220	YA862C15R	YA865C15R	YA868C15R
	TO-220F	YG862C15R	YG865C15R	YG868C15R
	T-Pack(D2)	TS862C15	TS865C15	—
	TFP	MS862C15	MS865C15	—
	TO-240	—	PH865C15	—
250	TO-220	YA872C25R*	YA875C25R*	—
	TO-220F	YG872C25R*	YG875C25R*	—
	T-Pack(D2)	TS872C25*	TS875C25*	—
	TFP	MS872C25*	MS875C25*	—
	TO-247	—	PH875C25*	—

* 试验性额定值 Tentative ratings